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Attorney Docket: F0056/1663P
PATENT

Transmitted herewith for filing is the Patent Application of

Inventors: **Zoran Krivokapic**

For: **METHOD AND SYSTEM FOR FORMING A LONG CHANNEL DEVICE**

Enclosed with the Patent Application are:

X Six (6) sheet(s) of drawings
X Declaration of Inventor(s)
X Power of Attorney by Assignee
X Assignment and Recordation Form
__ Information Disclosure Statement (PTO Form 1449)
X Self Addressed, Stamped Postcard

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Respectfully submitted,

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Attorney Docket: F0056/1663P

UNITED STATES PATENT APPLICATION

FOR

METHOD AND SYSTEM FOR FORMING A LONG CHANNEL DEVICE

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METHOD AND SYSTEM FOR FORMING A LONG CHANNEL DEVICE

FIELD OF THE INVENTION

The present invention relates to analog circuitry and more particularly to a technique for improving the performance of long channel devices.

BACKGROUND OF THE INVENTION

Semiconductor manufacturers have increasingly turned to high-density Metal Oxide Semiconductor (MOS) arrays in their integrated circuit design schemes. To achieve a high-density integrated circuit, features such as metal-oxide semiconductor field-effect transistors (MOSFETs) must be as small as possible. Integrated circuit device geometries well below one micron feature sizes continue to become increasingly common. In general, the use of smaller devices on integrated circuit chips results in better performance and high packing density, thereby reducing cost while increasing performance. However, with such small feature sizes, device performance is significantly impacted by physical effects which can be largely ignored with larger devices.

Small geometry devices exhibit a severe short channel effect, which manifests as a rapid drop of threshold voltage with decreasing channel length. In order to prevent subsurface leakage between source and drain, which is not controlled by the gate bias, one has to increase the dopant concentration of the channel. The side effect of this is that this dopant increase severely reduces drive currents. In order to avoid this problem halo or pocket implant are used since they don't increase the channel resistance but are strategically placed to raise the potential barrier between the source and drain.

Halo/pocket implants are moderately doped implants of the same conductivity type at

the well or substrate in which the transistor is formed, and which lie in a thin layer generally along the source/drain to substrate/well junctions. A combination of LDD structures and halo/pocket implants has proven to achieve good device performance and reliability.

For an illustration of the conventional methodology please refer now to Figure 1. Figure 1 is a flowchart illustrating the conventional process steps for utilizing LDD structures and halo/pocket implants in the design of electric circuitry. First, a single continuous channel gate is provided within an active region on a substrate, via step 10. Next, halo/pocket and LDD implants are provided, via step 12. Figure 2 shows the conventional channel gate structure 20.

Although halo/pocket and LDD implants work well with digital applications, halo/pocket and LDD implants are not suitable for analog applications where the channel gate length exceeds .75 μm. This is because long channel gates that have undergone halo/pocket and LDD implants have a significantly smaller Early Voltage which is undesirable for analog circuits.

Early Voltage is a measure of the degree to which the base modulation effect (or *Early effect*, after the scientist who first correctly explained its basis) impacts the characteristics of a bipolar transistor. A large value of V_A (>100 V) is desired in analog circuits for two reasons:

1. The *open-circuit voltage* gain, $\mathbf{a_0}$ (defined as the small-signal low-frequency voltage gain in the common-emitter configuration), is approximately found from:

$$\mathbf{a_0 = q\, V_A/kT}$$

where **q** is the elementary charge constant, **k** is the Boltzmann constant and **T** is temperature. Since $\mathbf{a_0}$ is the maximum voltage gain that can be obtained from a biolar

transistor, it is a significant parameter in analog circuits. Because the above referenced equation indicates that $\mathbf{a_0}$ depends only on $\mathbf{V_A}$ and T, a large value of $\mathbf{V_A}$ will permit larger voltage gains to be achieved.

2. Since $\Delta V_{CE} / \Delta I_C = V_A / I_C = r_0$ (where r_0 is the small-signal output resistance of the transistor in the common-emitter configuration), small values of V_A imply a smaller output resistance, which is generally undesirable. Analog applications therefore require a minimum V_A of 30 volts, while a lower voltage is normally acceptable for digital applications (15-20).

Figure 3 shows a conventional plot of the Early Voltage, V_A, vs. the channel length, L_{poly}. As can be seen in Figure 3, a device with a halo/pocket implant has a substantially lower V_A than a device without a halo/pocket implant.

The halo/pocket implant results in a barrier at both ends of the channel and these barriers inhibit current flow. Increasing the drain voltage has the effect of reducing the barrier at the drain end of the transistor and increasing the current. This results in a high output conductance value for the analog circuit. Since amplifier gain, G, is measured as

G = transconductance/output conductance

a high output conductance value results in a low amplifier gain. Consequently, because of the low amplifier gain, it is difficult to design useful analog applications.

Accordingly, what is needed is a system and method that allows for the effective use of halo/pocket and LDD implants in the design of analog circuitry without the aforementioned problems. The system and method should be easy to implement and cost effective. The present invention addresses such a need.

SUMMARY OF THE INVENTION

The present invention is a method of forming a channel device. The method comprises the steps of providing at least one active region on a substrate wherein the active region comprises a plurality of discontinuous gate structures. The method further comprises providing an ion implantation in the substrate.

In accordance with the present invention, a higher Early Voltage is achieved thereby enabling halo/pocket and LDD implants to be effectively utilized in the design of analog circuitry.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a flow chart illustrating the conventional process steps for utilizing LDD and halo/pocket implants in the design of electric circuitry.

Figure 2 shows the conventional channel gate structure.

Figure 3 shows a conventional plot of the Early Voltage, V_A, vs. the channel length, L_{poly}.

Figure 4 is a flowchart of the method in accordance with the present invention.

Figure 5 shows a structure in accordance with the present invention.

Figure 6 shows a plot of the Early Voltage, V_A, vs. the channel length, L_{poly}.

DETAILED DESCRIPTION

The present invention relates to a method and system for forming a long channel device. The following description is presented to enable one of ordinary skill in the art to make and use the invention and is provided in the context of a patent application and its

requirements. Various modifications to the preferred embodiment and the generic principles and features described herein will be readily apparent to those skilled in the art. Thus, the present invention is not intended to be limited to the embodiment shown but is to be accorded the widest scope consistent with the principles and features described herein.

The present invention is disclosed in the context of a preferred embodiment. The preferred embodiment of the present invention provides for a method for forming long channel devices in the design of analog circuitry. The method comprises dividing the channel gate into stacked structures of minimum channel length. Furthermore, the divided minimum channel length gates are connected at the metal level to the same gate voltage. Since the channel is inverted only under the stacked structures of minimum channel length, the degradation of the transistor parameters (i.e. threshold voltage, transconductance) is minimized. By minimizing the degradation of the transistor parameters, halo/pocket and LDD implants can be effectively utilized in the design of analog circuitry. Specifically, through the use of the method/system in accordance with the present invention, an Early Voltage higher than that of the conventional methodology is achieved thereby improving the performance of the resulting analog circuit.

For a better understanding of the method in accordance with the present invention, please refer to the flowchart of Figure 4. Firstly, at least one active region is provided on a substrate wherein the active region comprises a plurality of discontinuous gate structures, via step 100. The plurality of gate structures comprises three (3) gate structures of minimum channel length with nominal spacing therebetween. These structures are subsequently connected at the metal level to the same gate voltage. Preferably, for the 0.18μm technology, the minimum gate length is 0.18μm with a 0.27μm spacing therebetween and for the 0.13μm technology, the minimum gate length is 0.13μm with a 0.2μm spacing therebetween. Next, ion

implantation is provided, via step 102. Preferably, the ion implantation comprises halo/pocket and lightly doped drain implants. Furthermore, the gate structures are preferably masked prior to the performance of the halo/pocket and LDD implants. Since the channel is inverted only under the stacked structures of minimum channel length, the detrimental effect on the Early Voltage due to the performance of the halo/pocket and LDD implants is substantially reduced.

For a further illustration of the present invention, please refer to Figure 5. Figure 5 shows a structure 200 in accordance with the present invention. The structure comprises a plurality of gate structures 204 of minimal length on a substrate 206. As previously stated, the gate structures 204 are provided with a mask 202 prior to the performance of the LDD and halo/pocket implants.

Figure 6 shows a plot of the Early Voltage, V_A, vs. the channel length, L_{poly}. As can be seen in Figure 6, a device with a halo/pocket implant that incorporates the method in accordance with the present invention has a substantially higher V_A than a device with a halo/pocket implant that does not incorporate the method in accordance with the present invention.

Through the use of the method/system in accordance with the present invention, the degradation of the transistor parameters (i.e. threshold voltage, transconductance) is minimized. By minimizing the degradation of the transistor parameters, a higher Early Voltage is achieved thereby enabling halo/pocket and LDD implants to be effectively utilized in the design of analog circuitry.

A method and system for forming a channel gate is disclosed. Although the present invention has been described in accordance with the embodiments shown, one of ordinary skill in the art will readily recognize that there could be variations to the embodiments and those

variations would be within the spirit and scope of the present invention. Accordingly, many modifications may be made by one of ordinary skill in the art without departing from the spirit and scope of the appended claims.

CLAIMS

What is claimed is:

1. A method for forming a channel device comprising the steps of:

a) providing at least one active region on a substrate wherein the active region comprises a plurality of discontinuous gate structures; and

b) providing an ion implantation in the substrate.

2. The method of claim 1 wherein step b) further comprises:

b1) masking the plurality of gate structures prior to the ion implantation.

3. The method of claim 2 wherein the active region comprises three gate structures.

4. The method of claim 3 wherein each of the three gate structures comprises a channel length of at least 0.13μm disposed at least 0.2μm apart.

5. The method of claim 1 wherein the ion implantation comprises a lightly doped drain implant.

6. The method of claim 5 wherein the ion implantation further comprises a halo implant.

7. The method of claim 5 wherein the ion implantation further comprises a pocket implant.

8. The method of claim 1 wherein each of the plurality of discontinuous gate structures are connected to a gate voltage source.

9. A system for forming a channel device comprising:

means for providing at least one active region on a substrate wherein the active region comprises a plurality of gate structures; and

means for providing an ion implantation in the substrate.

10. The system of claim 9 wherein means for providing the ion implantation further comprises:

means for masking the plurality of gate structures prior to the ion implantation.

11. The system of claim 10 wherein the active region comprises three gate structures.

12. The system of claim 11 wherein each of the three gate structures comprises a channel length of at least 0.13μm disposed at least 0.2μm apart.

13. The system of claim 10 wherein the ion implantation comprises a lightly doped drain implant.

14. The system of claim 13 wherein the ion implantation further comprises a halo implant.

15. The system of claim 13 wherein the ion implantation further comprises a pocket implant.

16. The system of claim 9 wherein each of the plurality of discontinuous gate structures are connected to a gate voltage source.

ABSTRACT

The present invention is a method of forming a channel device. The method comprises the steps of providing at least one active region on a substrate wherein the active region comprises a plurality of discontinuous gate structures. The method further comprises providing an ion implantation in the substrate. In accordance with the present invention, a higher Early Voltage is achieved thereby enabling halo/pocket and LDD implants to be effectively utilized in the design of analog circuitry.

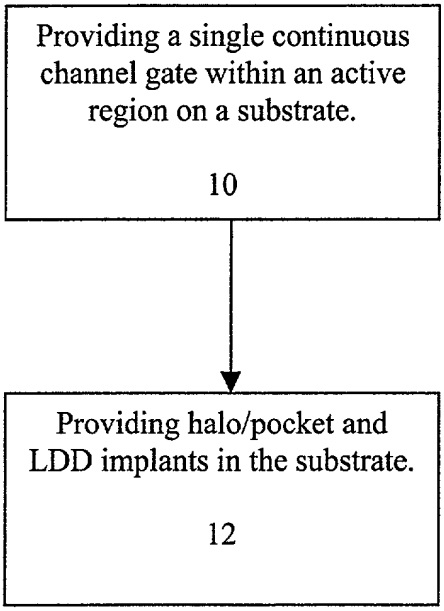

Figure 1
Prior Art

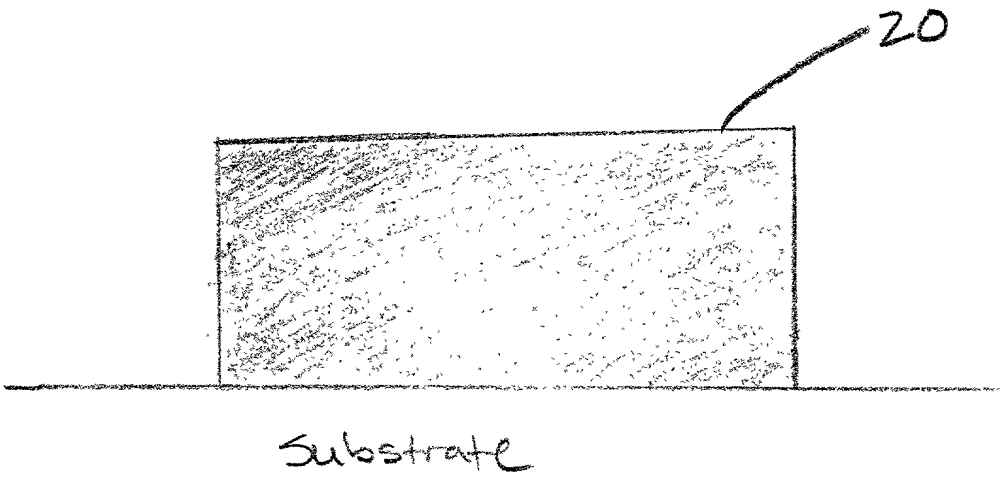

Figure 2
Prior Art

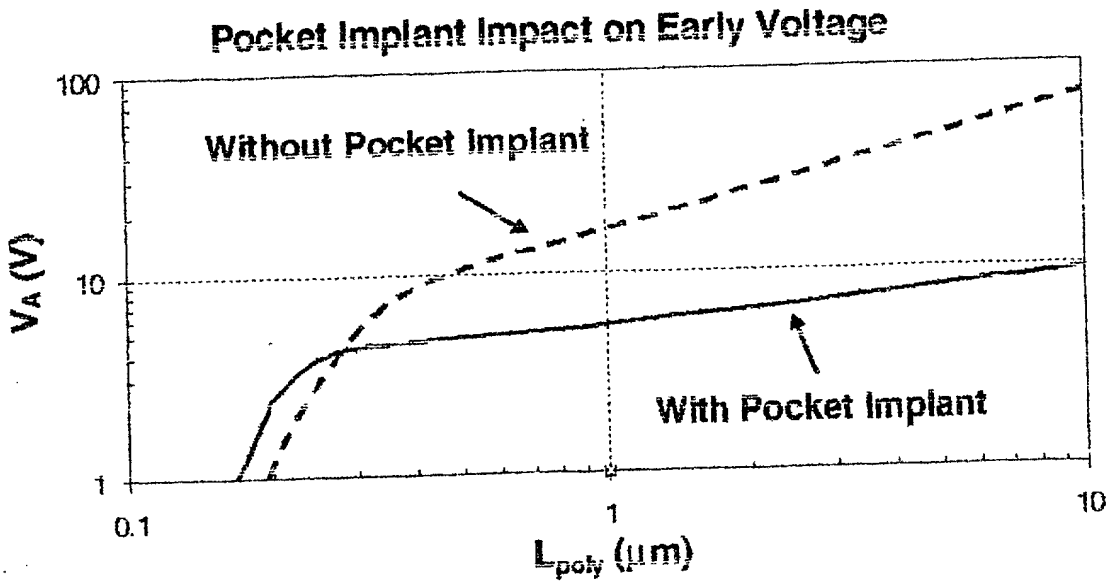

Figure 3
Prior Art

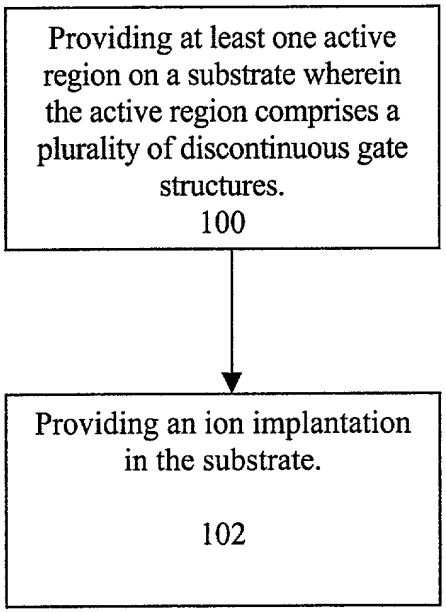
Providing at least one active region on a substrate wherein the active region comprises a plurality of discontinuous gate structures.
100
Providing an ion implantation in the substrate.
102

Figure 4

200

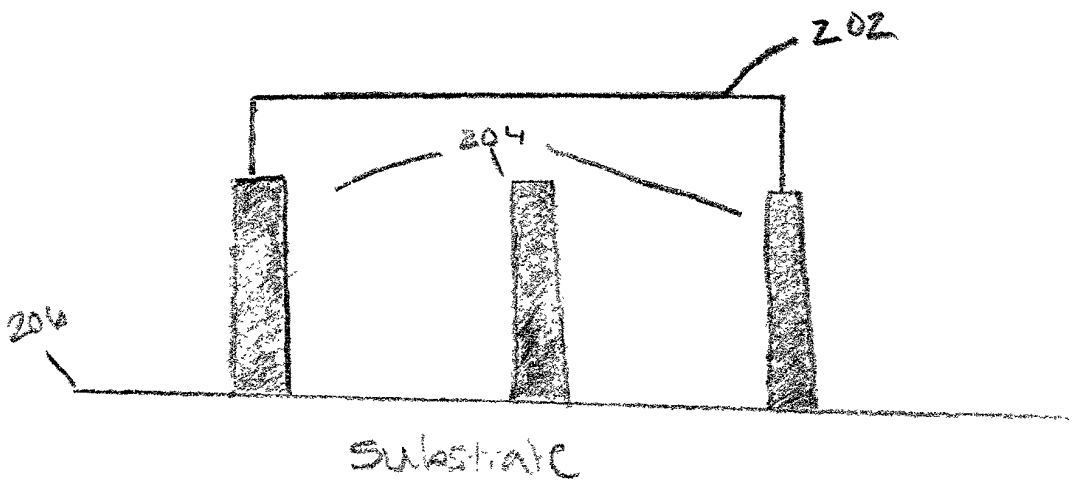

Figure 5

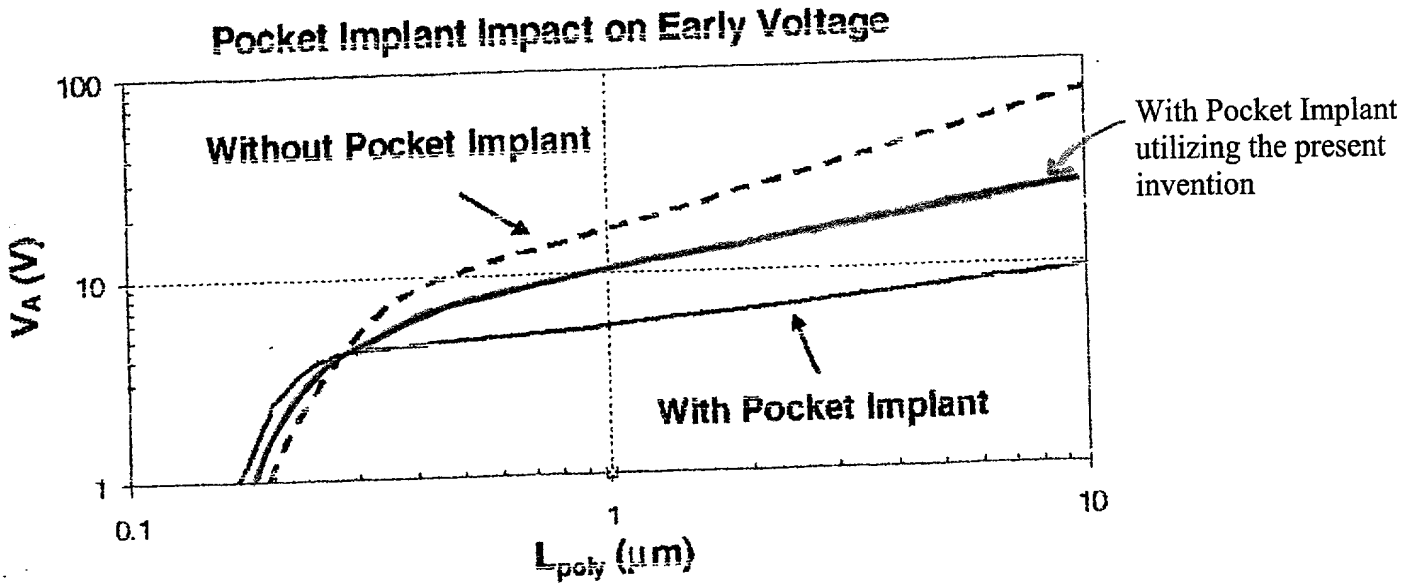
Pocket Implant Impact on Early Voltage
100
10
1
0.1
1
10
V_A (V)
L_{poly} (µm)
Without Pocket Implant
With Pocket Implant
With Pocket Implant utilizing the present invention

Figure 6

DECLARATION

As the below named join-inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name; that I verily believe I am the first, original and joint-inventor of the invention entitled:

METHOD AND SYSTEM FOR FORMING A LONG CHANNEL DEVICE

described and claimed in the specification which is attached hereto that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above; that I do not know and do not believe the same was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months prior to this application, that I acknowledge my duty to disclose information of which I am aware that is material to the examination of this application as defined by 37 C.F.R. ɔ1.56, and that no application for patent or inventor's certificate on said invention has been filed in any country foreign to the United States of America by my or by my legal representatives or assigns.

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Citizenship: **United States of America**

6/2/00
Date

Signature of Inventor

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of: **Zoran Krivokapic**

Title: **METHOD AND SYSTEM FOR FORMING A LONG CHANNEL DEVICE**

POWER OF ATTORNEY BY ASSIGNEE
AND EXCLUSION OF INVENTOR UNDER 37 C.F.R. SEC. 1.32

Honorable Commissioner of Patents and Trademarks
Box Patent Applications
Washington, D.C. 20231

Sir:

ADVANCED MICRO DEVICES, Inc., a Delaware Corporation, having become the owner of all rights in and to the above-identified application by virtue of an Assignment executed by the inventor concurrently with the execution of the application, said Assignment being submitted herewith for recording, hereby appoints:

Vincenzo D. Pitruzzella, Reg. No. 28,656
Richard J. Roddy, Reg. No. 27,688
William D. Zahrt, II, Reg. No. 26,070
Paul S. Drake, Reg. No. 33,491
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their attorneys, to prosecute said application and to transact in connection therewith all business in the Patent and Trademark Office and before competent International Authorities; said appointment to be to the exclusion of the inventor and his attorneys in accordance with the provisions of 37 C.F.R. 1.32.

Date: June 8, 2000

Name: Richard J. Roddy

Title: Chief Patent and Trademark Counsel